WRITING TO

FERROELECTRIC MEMORY DEVICES

RELATED APPLICATIONS

[0001] This application is a divisional of United States Patent Application Serial No. 10/205,989 filed July 26, 2002 and titled, "Array Architecture for Depletion Mode Ferroelectric Memory Devices" ~~(allowed)~~, now patent no. 6,665,206 which application is commonly assigned and incorporated herein by reference, and which is a divisional of United States Patent Application Serial No. 09/653,074 filed August 31, 2000 titled, "Array Architecture for Depletion Mode Ferroelectric Memory Devices," issued as US 6,587,365 on July 1, 2003.

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TECHNICAL FIELD OF THE INVENTION

[0002] The present invention relates to ferroelectric memory devices, and particularly to memory array architectures making use of ferroelectric depletion-mode field-effect transistors.

BACKGROUND OF THE INVENTION

[0003] Ferroelectric materials are a class of materials that can be thought of as having electrical properties somewhat analogous to the magnetic properties of ferromagnetic materials. A uniaxial ferromagnetic material can be magnetized in one of two directions, and thereafter will retain a magnetic field in that direction even after the applied magnetic field is removed; similarly, a ferroelectric material can be "polarized" in either direction (by applying an electric field to it), and thereafter will retain an electric field in that direction, even after the applied electric field is removed.

[0004] Ferroelectric materials have been successfully integrated into integrated circuit processes, but this integration can have some drawbacks. Ferroelectric materials having sufficient thermal stability for integrated circuit processing often include incompatible metals that must be separated from a silicon substrate. Such ferroelectric materials also tend to be strong oxygen sources, increasing the risk of undesirable